FIG. 1

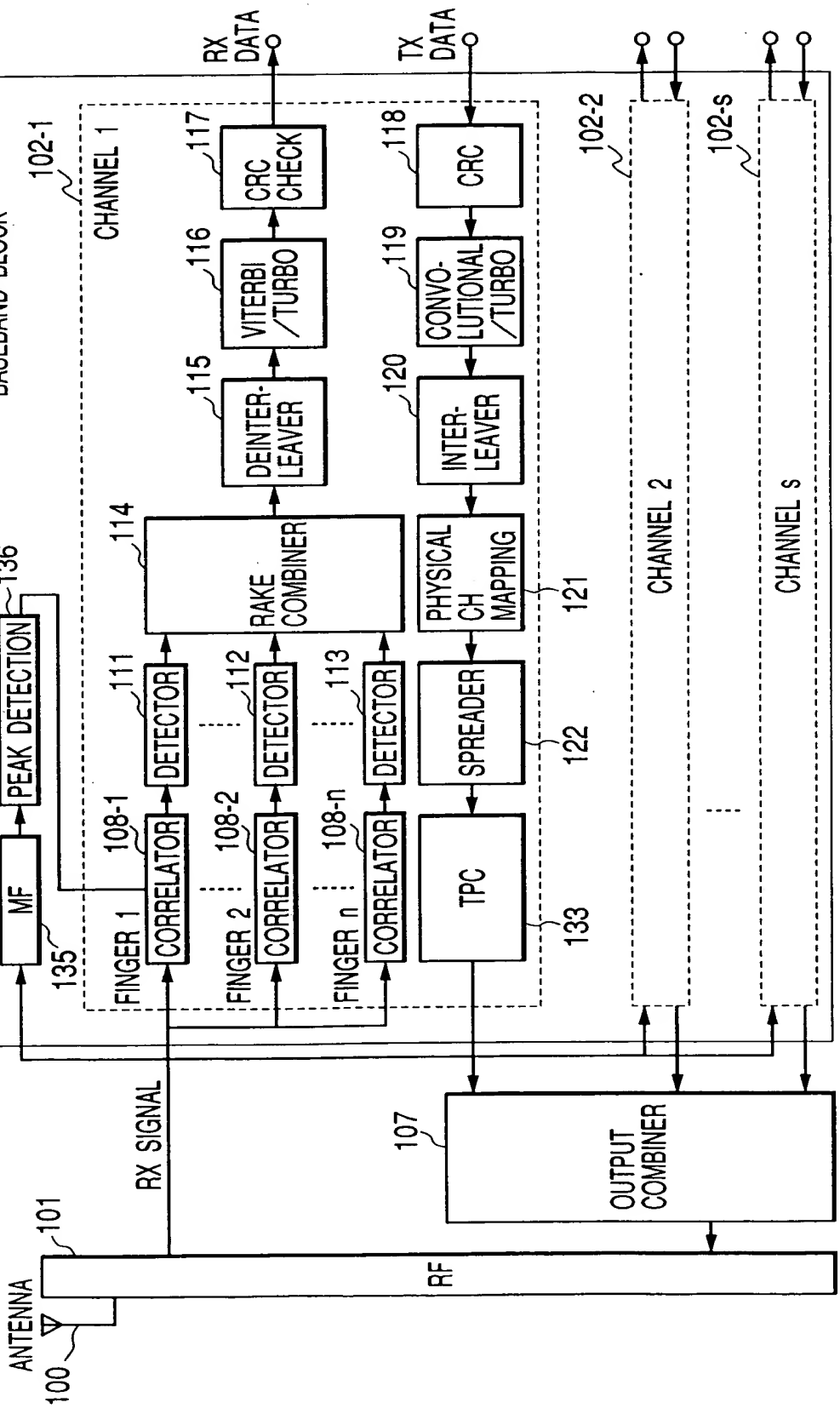

ANTENNA
100
101
RF
RX SIGNAL
BASEBAND BLOCK
134
MF
135
PEAK DETECTION
136
FINGER 1
FINGER 2
FINGER n
CORRELATOR
108-1
108-2
108-n
DETECTOR
111
112
113
RAKE COMBINER
114
DEINTER-LEAVER
115
VITERBI /TURBO
116
CRC CHECK
117
RX DATA
CHANNEL 1
102-1
CHANNEL 2
102-2
CHANNEL s
102-s
TX DATA
CRC
118
CONVO-LUTIONAL /TURBO
119
INTER-LEAVER
120
PHYSICAL CH MAPPING
121
SPREADER
122
TPC
133
OUTPUT COMBINER
107

FIG. 2

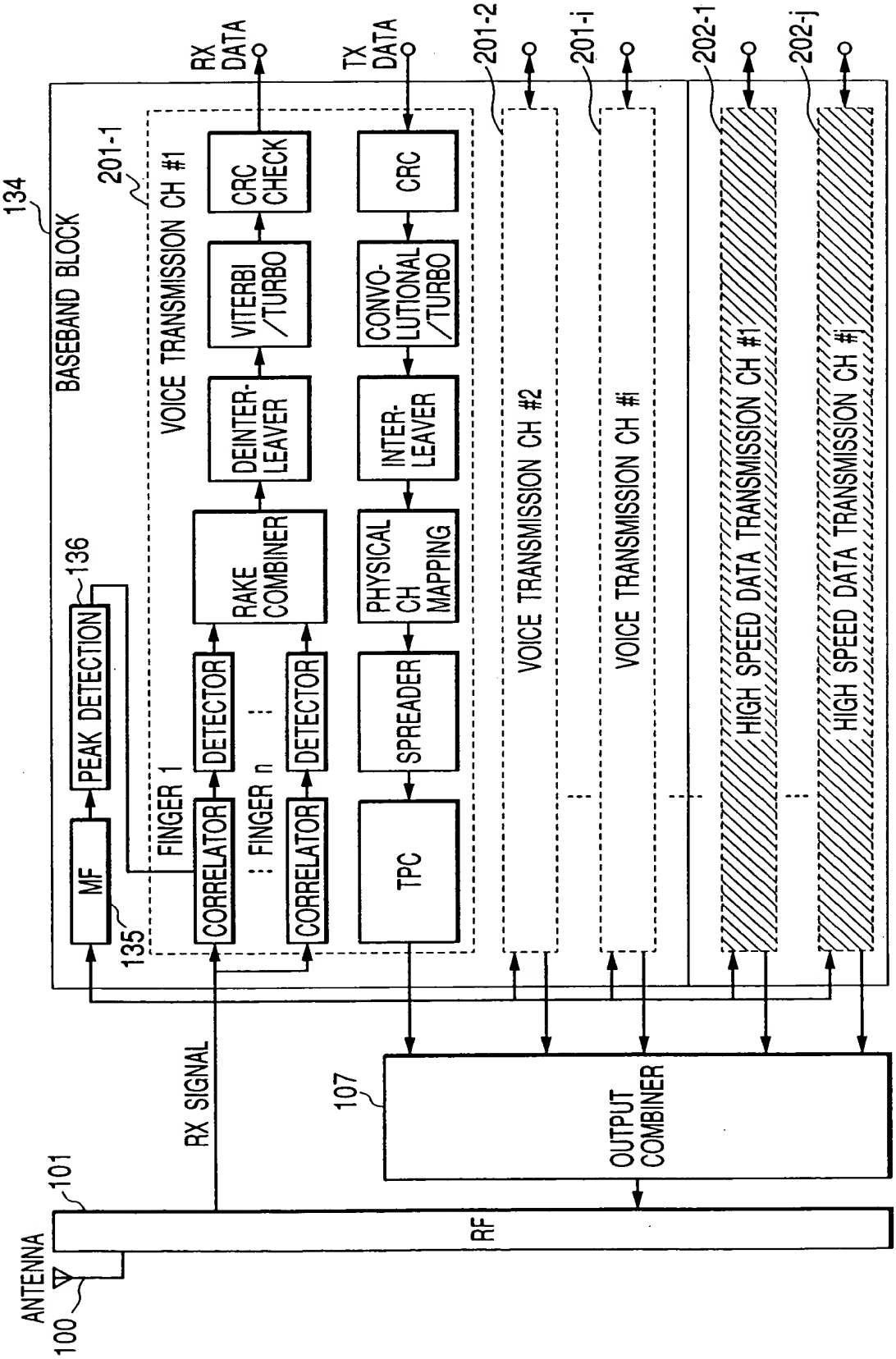

ANTENNA
100
101
RF
RX SIGNAL
107
OUTPUT COMBINER
134
BASEBAND BLOCK
135
MF
PEAK DETECTION
136
FINGER 1
FINGER n
CORRELATOR
DETECTOR
RAKE COMBINER
DEINTER-LEAVER
VITERBI /TURBO
CRC CHECK
RX DATA
TPC
SPREADER
PHYSICAL CH MAPPING
INTER-LEAVER
CONVO-LUTIONAL /TURBO
CRC
TX DATA
201-1
VOICE TRANSMISSION CH #1
201-2
VOICE TRANSMISSION CH #2
201-i
VOICE TRANSMISSION CH #i
202-1
HIGH SPEED DATA TRANSMISSION CH #1
202-j
HIGH SPEED DATA TRANSMISSION CH #j

FIG. 3

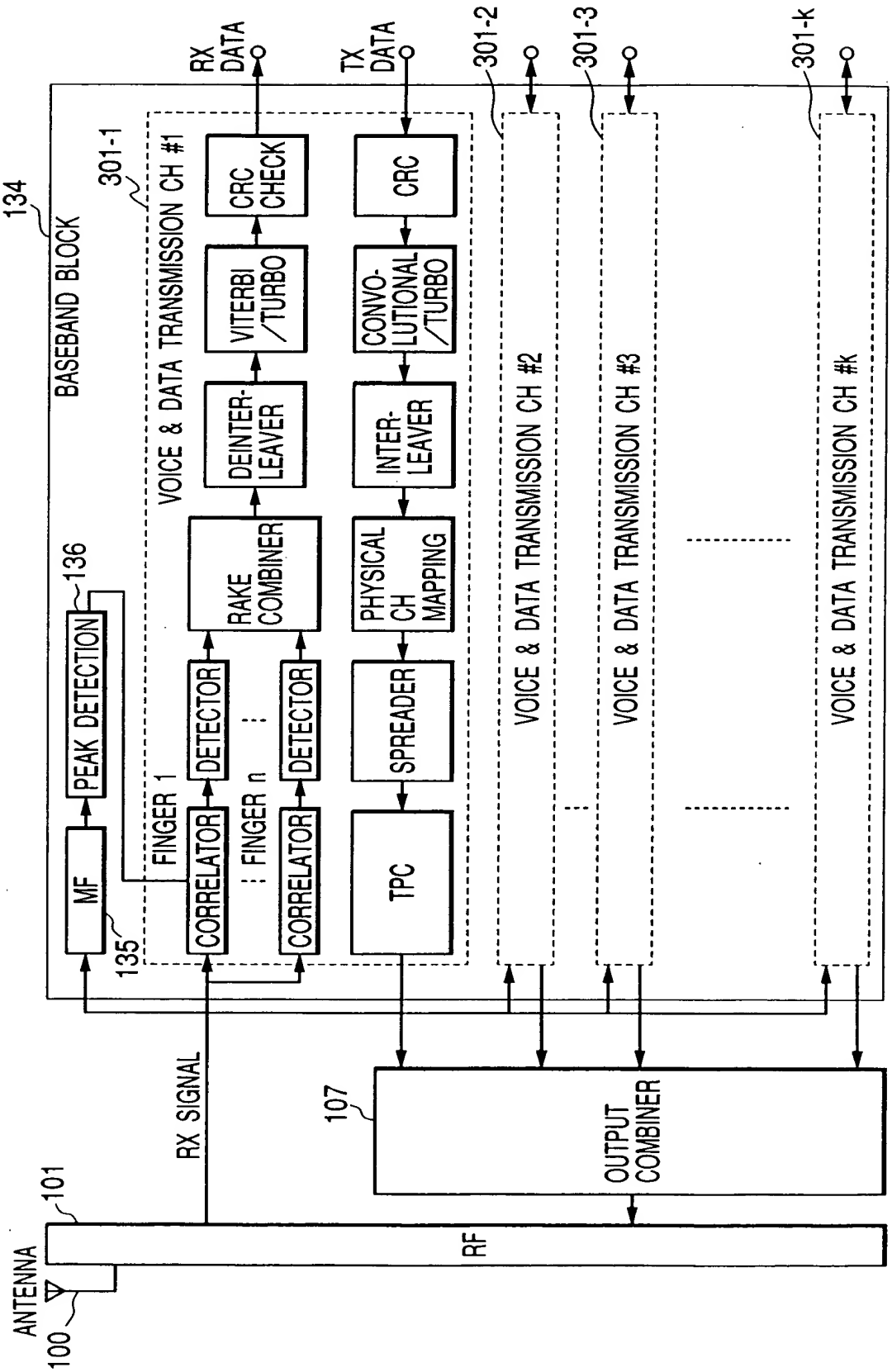

ANTENNA
100
101
RF
RX SIGNAL
107
OUTPUT COMBINER
134
BASEBAND BLOCK
301-1
VOICE & DATA TRANSMISSION CH #1
FINGER 1
FINGER n
MF
PEAK DETECTION
136
135
CORRELATOR
CORRELATOR
DETECTOR
DETECTOR
RAKE COMBINER
DEINTER-LEAVER
VITERBI /TURBO
CRC CHECK
RX DATA
TPC
SPREADER
PHYSICAL CH MAPPING
INTER-LEAVER
CONVO-LUTIONAL /TURBO
CRC
TX DATA
301-2
VOICE & DATA TRANSMISSION CH #2
301-3
VOICE & DATA TRANSMISSION CH #3
301-k
VOICE & DATA TRANSMISSION CH #k

FIG. 4

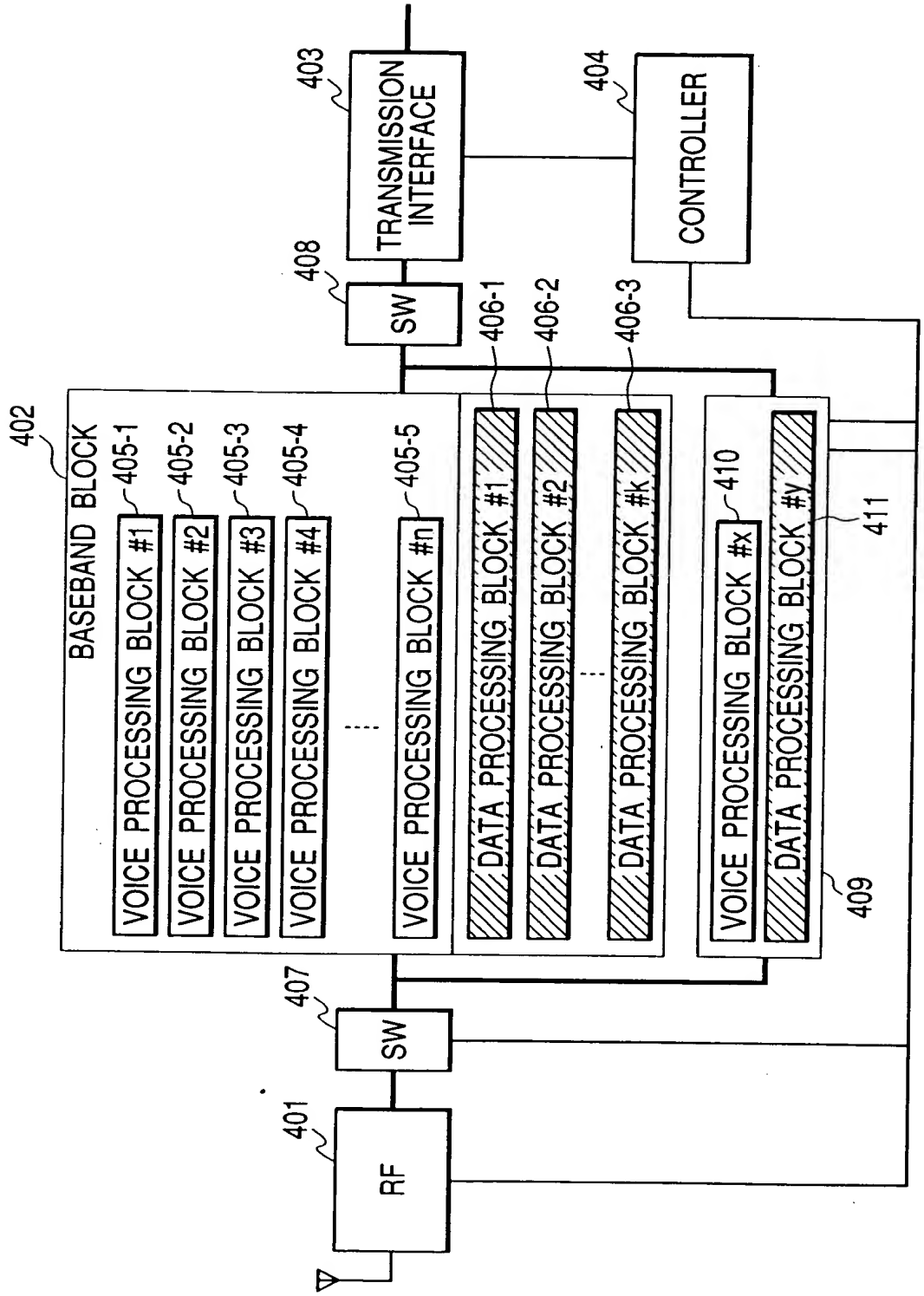

401
RF
407
SW
402
BASEBAND BLOCK
405-1
VOICE PROCESSING BLOCK #1
405-2
VOICE PROCESSING BLOCK #2
405-3
VOICE PROCESSING BLOCK #3
405-4
VOICE PROCESSING BLOCK #4
405-5
VOICE PROCESSING BLOCK #n
406-1
DATA PROCESSING BLOCK #1
406-2
DATA PROCESSING BLOCK #2
406-3
DATA PROCESSING BLOCK #k
410
VOICE PROCESSING BLOCK #x
411
DATA PROCESSING BLOCK #y
409
408
SW
403
TRANSMISSION INTERFACE
404
CONTROLLER

FIG. 5

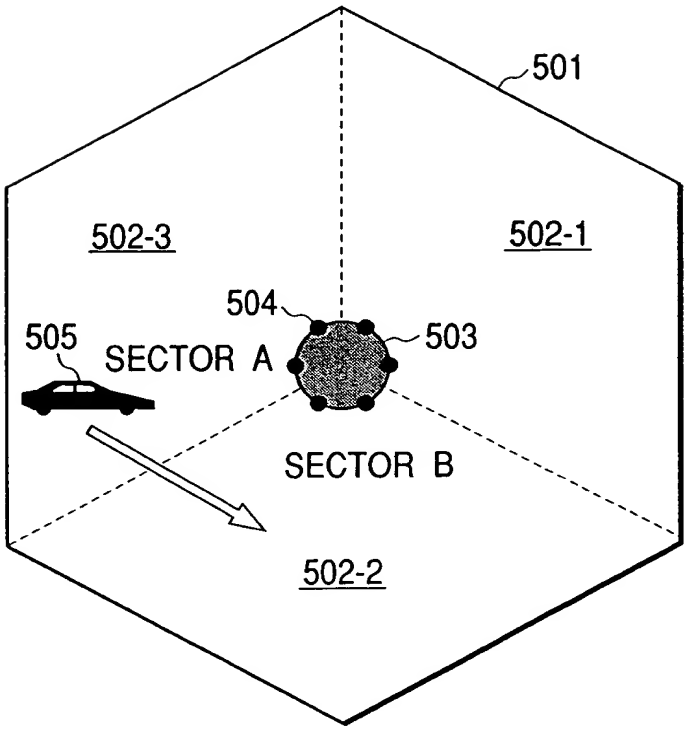

501
502-3
502-1
504
503
505
SECTOR A
SECTOR B
502-2

FIG. 6

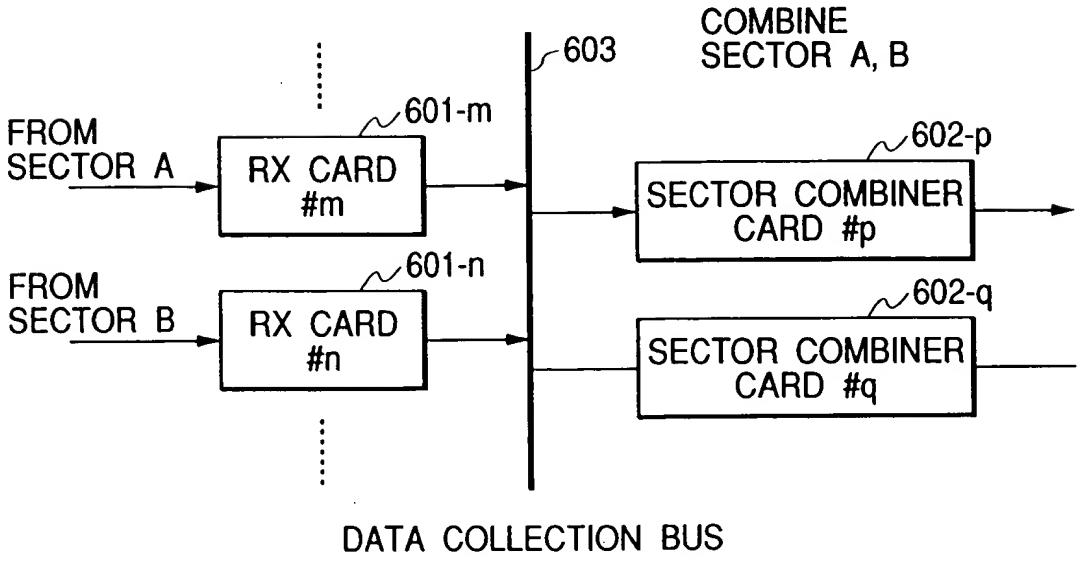

COMBINE
SECTOR A, B
603
601-m
FROM
SECTOR A
RX CARD
#m
602-p
SECTOR COMBINER
CARD #p
601-n
FROM
SECTOR B
RX CARD
#n
602-q
SECTOR COMBINER
CARD #q
DATA COLLECTION BUS

FIG. 7

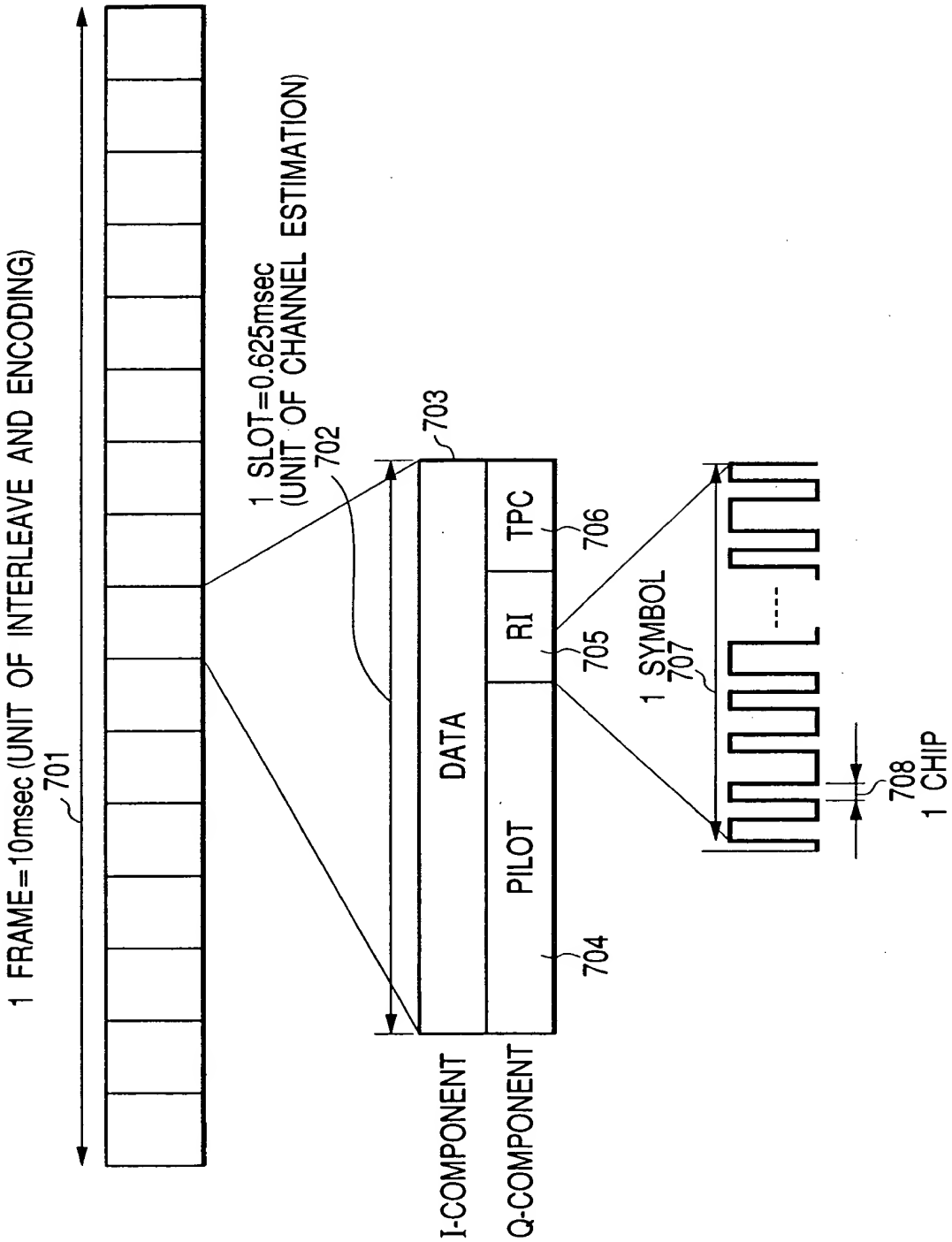

1 FRAME=10msec (UNIT OF INTERLEAVE AND ENCODING)
701
1 SLOT=0.625msec
(UNIT OF CHANNEL ESTIMATION)
702
703
DATA
TPC
RI
PILOT
706
705
704
I-COMPONENT
Q-COMPONENT
1 SYMBOL
707
708
1 CHIP

FIG. 8

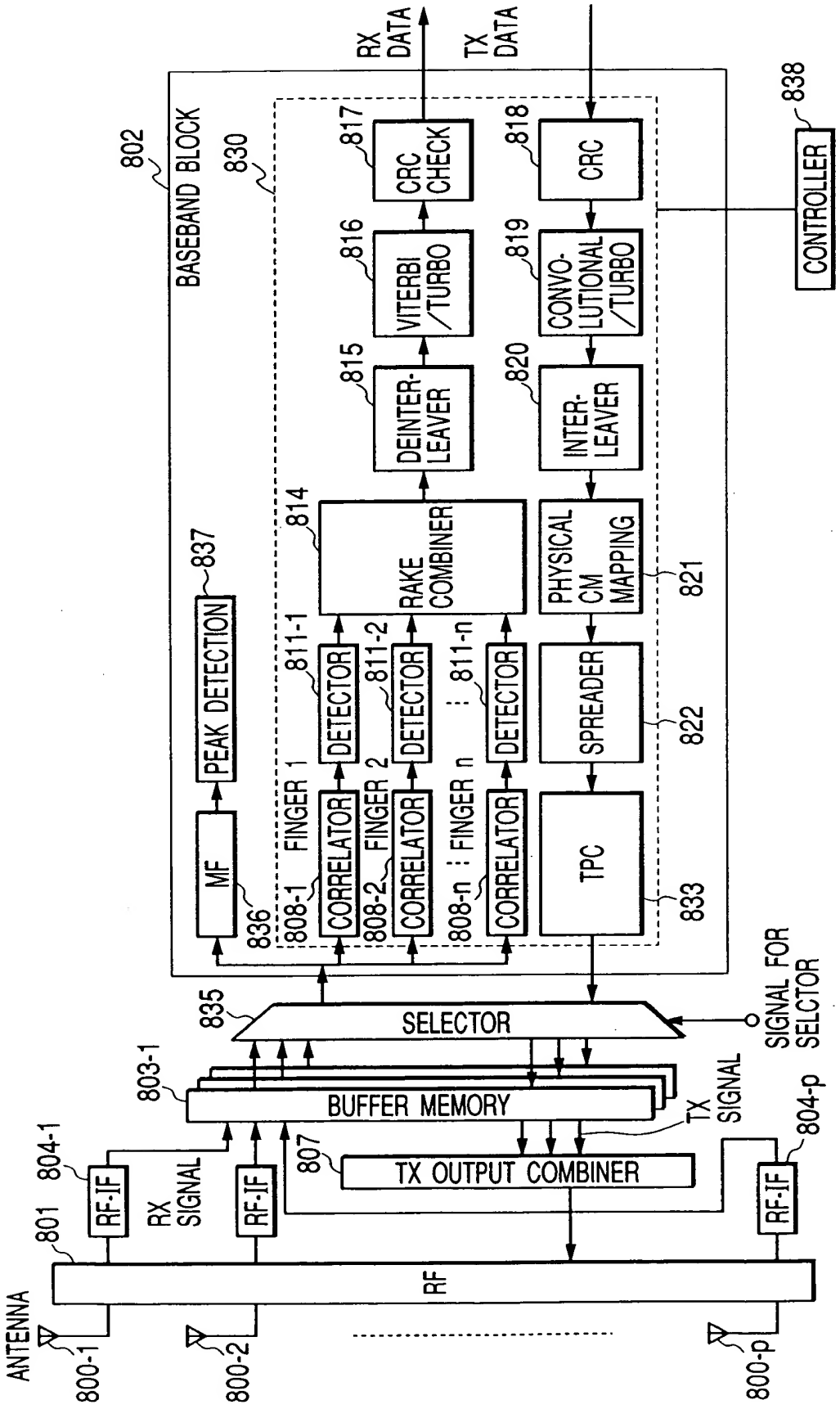

ANTENNA
800-1
800-2
800-p
801
RF
RF-IF
804-1
804-p
RX SIGNAL
TX SIGNAL
803-1
BUFFER MEMORY
807
TX OUTPUT COMBINER
835
SELECTOR
SIGNAL FOR SELCTOR
802
BASEBAND BLOCK
830
FINGER 1
FINGER 2
FINGER n
808-1
808-2
808-n
CORRELATOR
811-1
811-2
811-n
DETECTOR
814
RAKE COMBINER
815
DEINTER-LEAVER
816
VITERBI /TURBO
817
CRC CHECK
RX DATA
TX DATA
818
CRC
819
CONVO-LUTIONAL /TURBO
820
INTER-LEAVER
821
PHYSICAL CM MAPPING
822
SPREADER
833
TPC
836
MF
837
PEAK DETECTION
838
CONTROLLER

FIG. 9

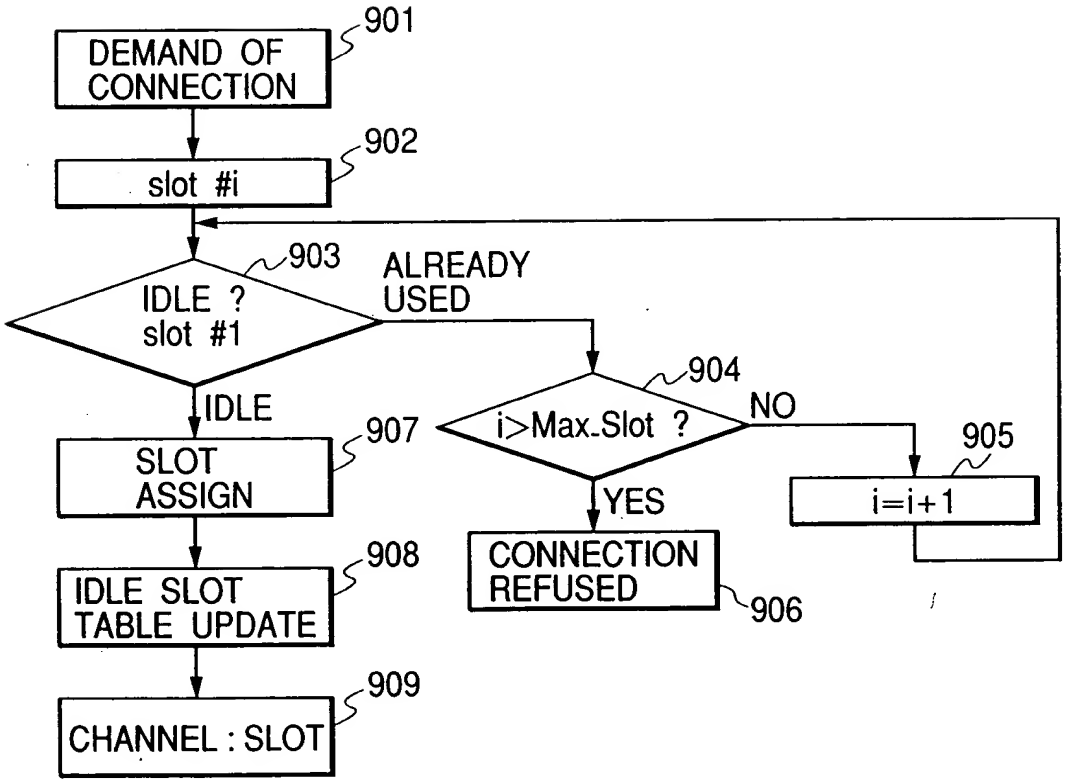

DEMAND OF CONNECTION
901
slot #i
902
IDLE ? slot #1
903
ALREADY USED
IDLE
SLOT ASSIGN
907
i>Max_Slot ?
904
NO
YES
905
i=i+1
CONNECTION REFUSED
906
IDLE SLOT TABLE UPDATE
908
CHANNEL : SLOT
909

FIG. 10

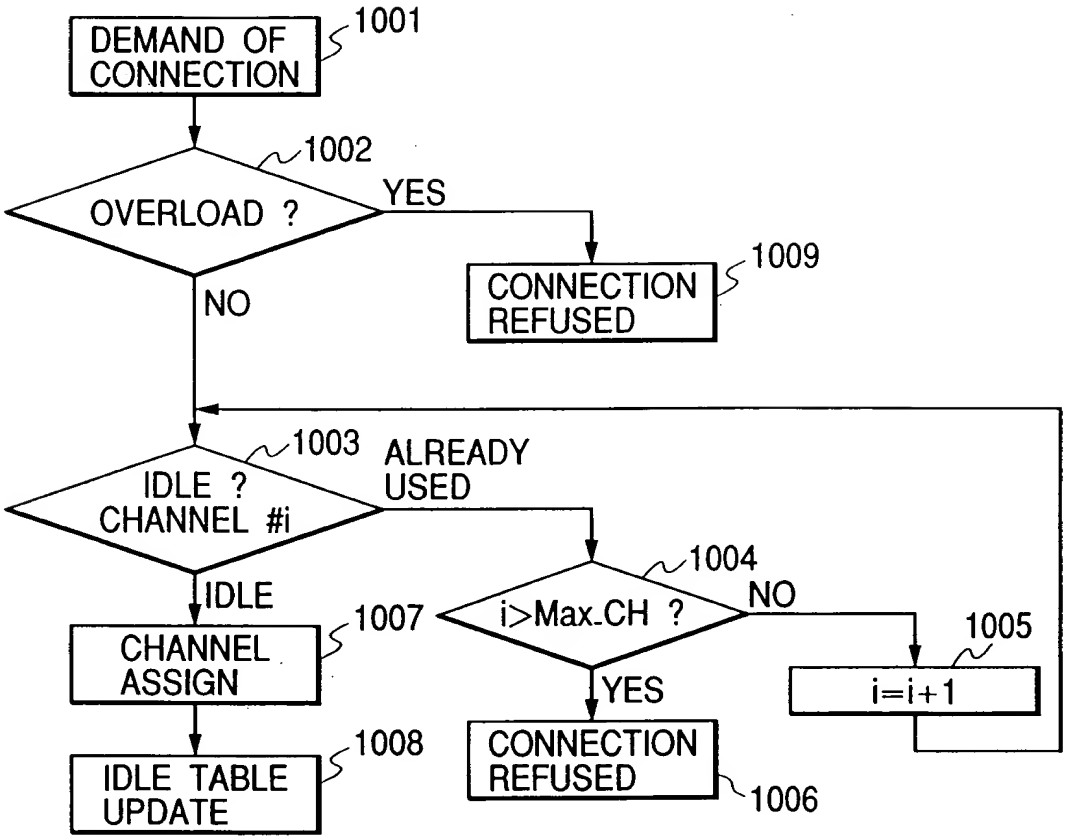

DEMAND OF CONNECTION
1001
OVERLOAD ?
1002
YES
CONNECTION REFUSED
1009
NO
IDLE ? CHANNEL #i
1003
ALREADY USED
IDLE
i>Max_CH ?
1004
NO
1005
i=i+1
YES
CHANNEL ASSIGN
1007
CONNECTION REFUSED
1006
IDLE TABLE UPDATE
1008

FIG. 11

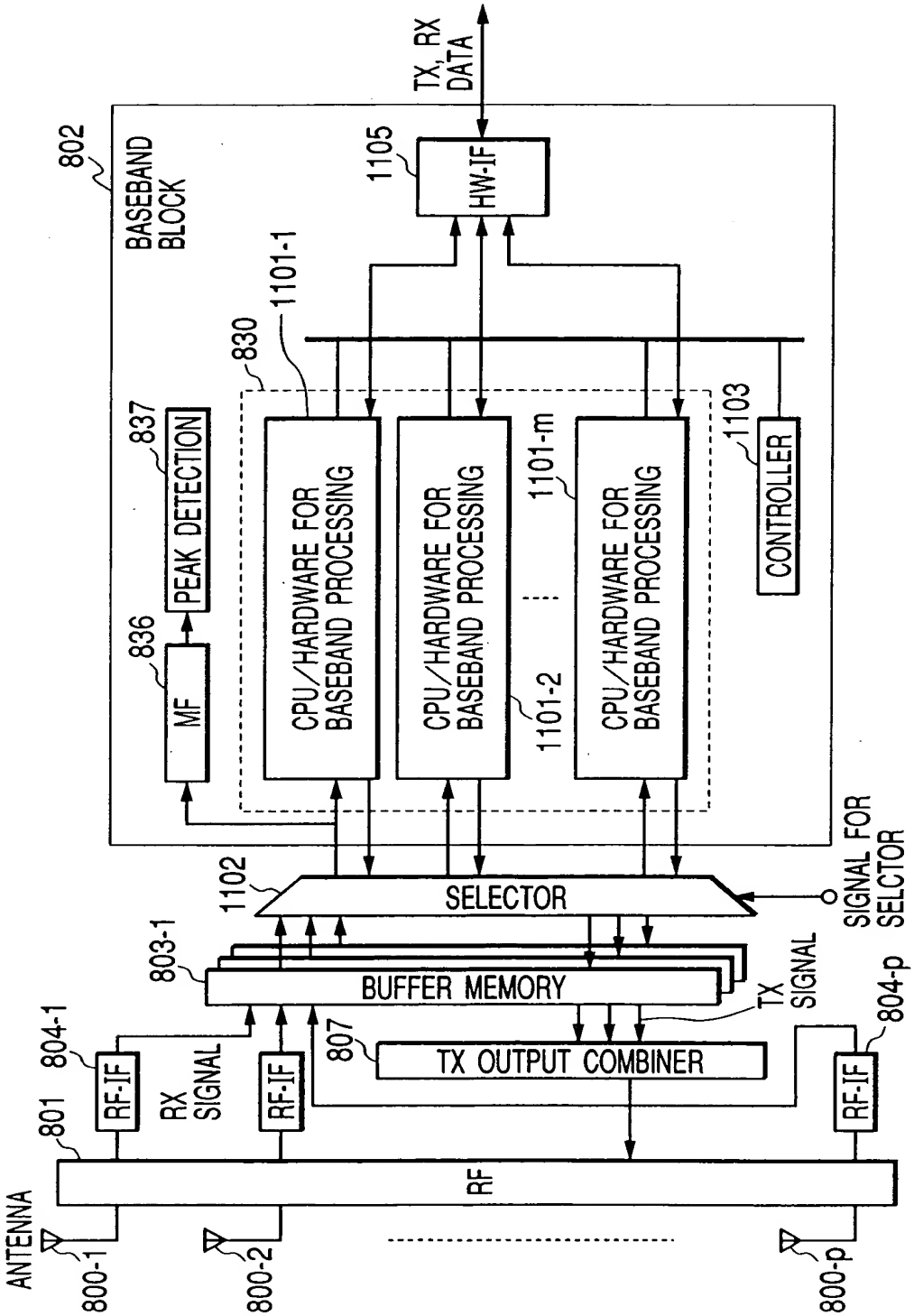

TX, RX DATA
802
BASEBAND BLOCK
1105
HW-IF
1101-1
830
837
PEAK DETECTION
836
MF
CPU/HARDWARE FOR BASEBAND PROCESSING
CPU/HARDWARE FOR BASEBAND PROCESSING
1101-m
1101-2
CPU/HARDWARE FOR BASEBAND PROCESSING
1103
CONTROLLER
1102
SELECTOR
SIGNAL FOR SELCTOR
803-1
BUFFER MEMORY
TX SIGNAL
804-p
804-1
RF-IF
RX SIGNAL
RF-IF
807
TX OUTPUT COMBINER
RF-IF
801
RF
ANTENNA
800-1
800-2
800-p

FIG. 12

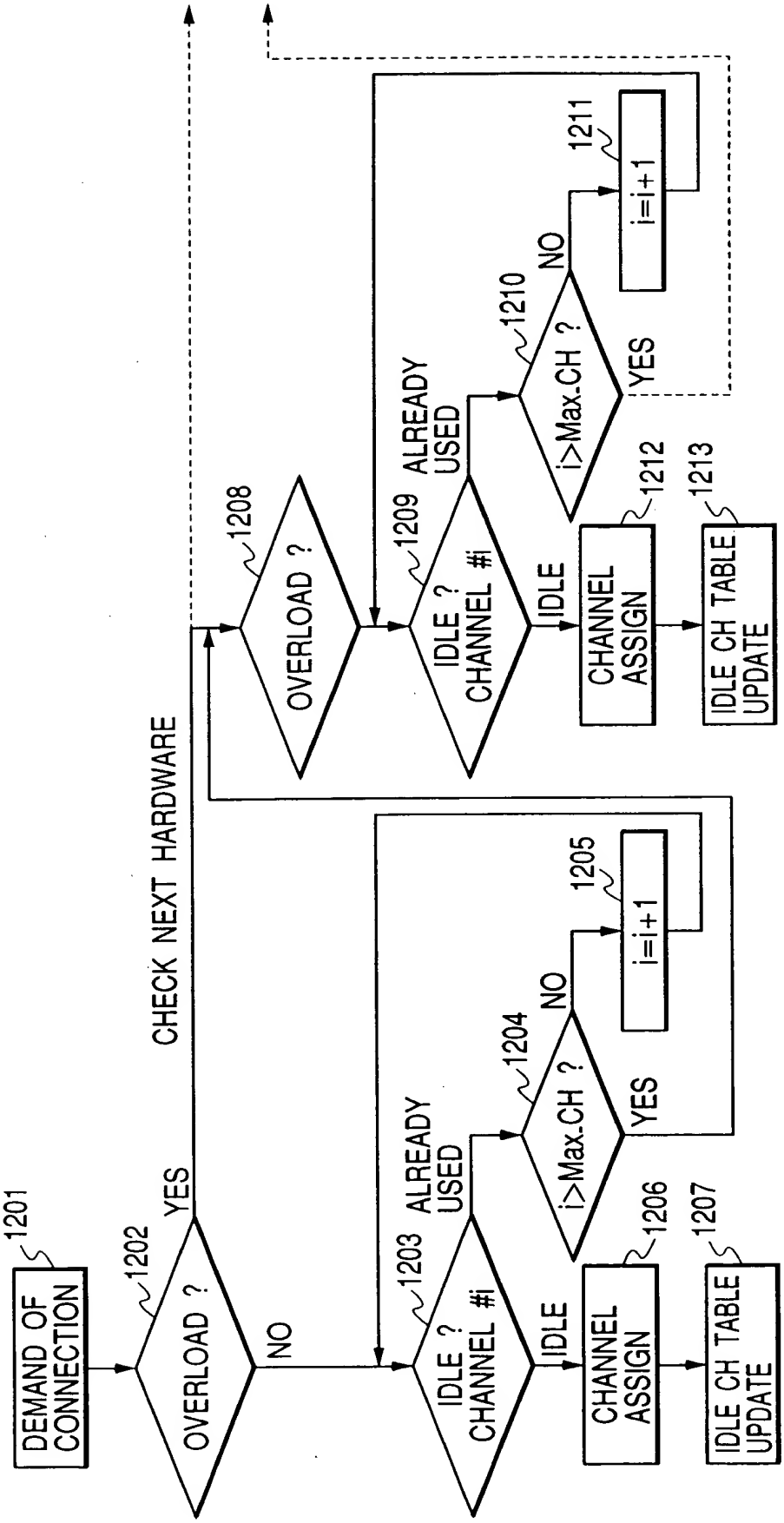

DEMAND OF CONNECTION
1201
OVERLOAD ?
1202
YES
NO
CHECK NEXT HARDWARE
IDLE ? CHANNEL #i
1203
ALREADY USED
i>Max.CH ?
1204
YES
NO
i=i+1
1205
IDLE
CHANNEL ASSIGN
1206
IDLE CH TABLE UPDATE
1207
OVERLOAD ?
1208
IDLE ? CHANNEL #i
1209
ALREADY USED
i>Max.CH ?
1210
YES
NO
i=i+1
1211
IDLE
CHANNEL ASSIGN
1212
IDLE CH TABLE UPDATE
1213

FIG. 13

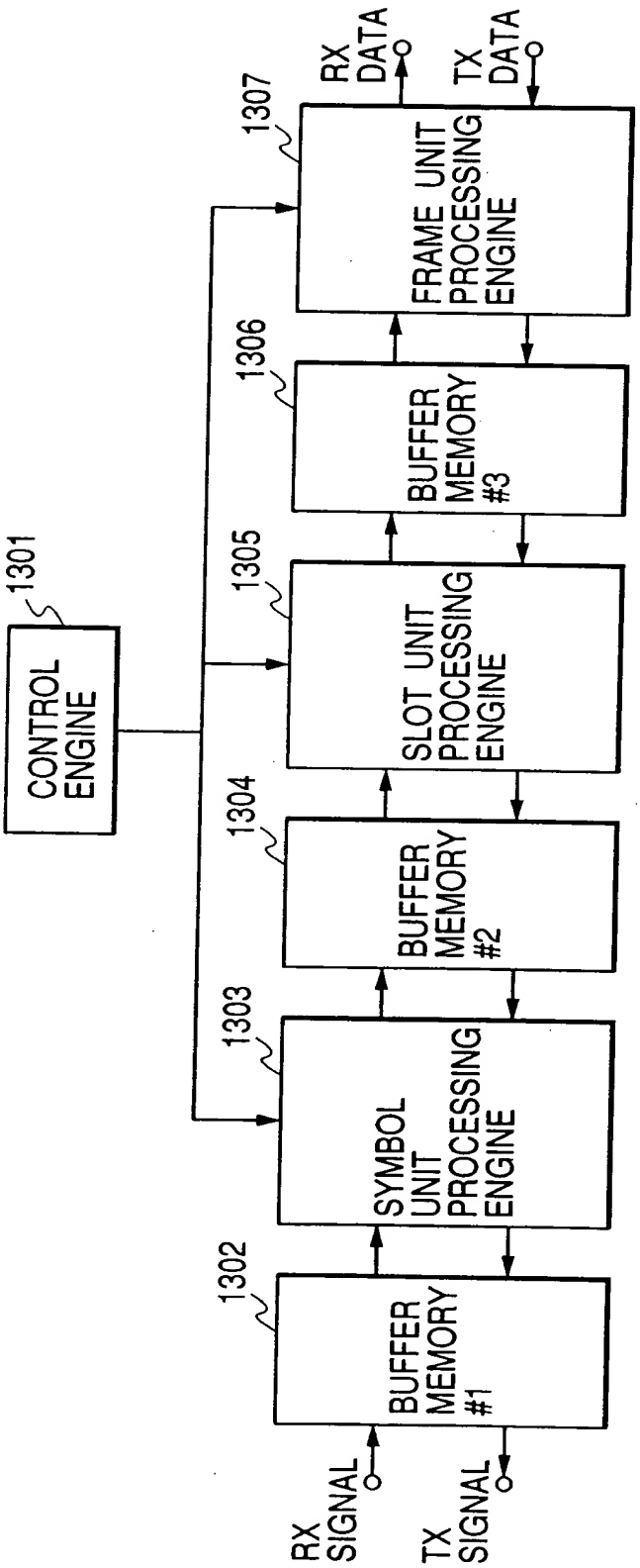

CONTROL ENGINE
1301
BUFFER MEMORY #1
1302
SYMBOL UNIT PROCESSING ENGINE
1303
BUFFER MEMORY #2
1304
SLOT UNIT PROCESSING ENGINE
1305
BUFFER MEMORY #3
1306
FRAME UNIT PROCESSING ENGINE
1307
RX SIGNAL
TX SIGNAL
RX DATA
TX DATA

FIG. 14

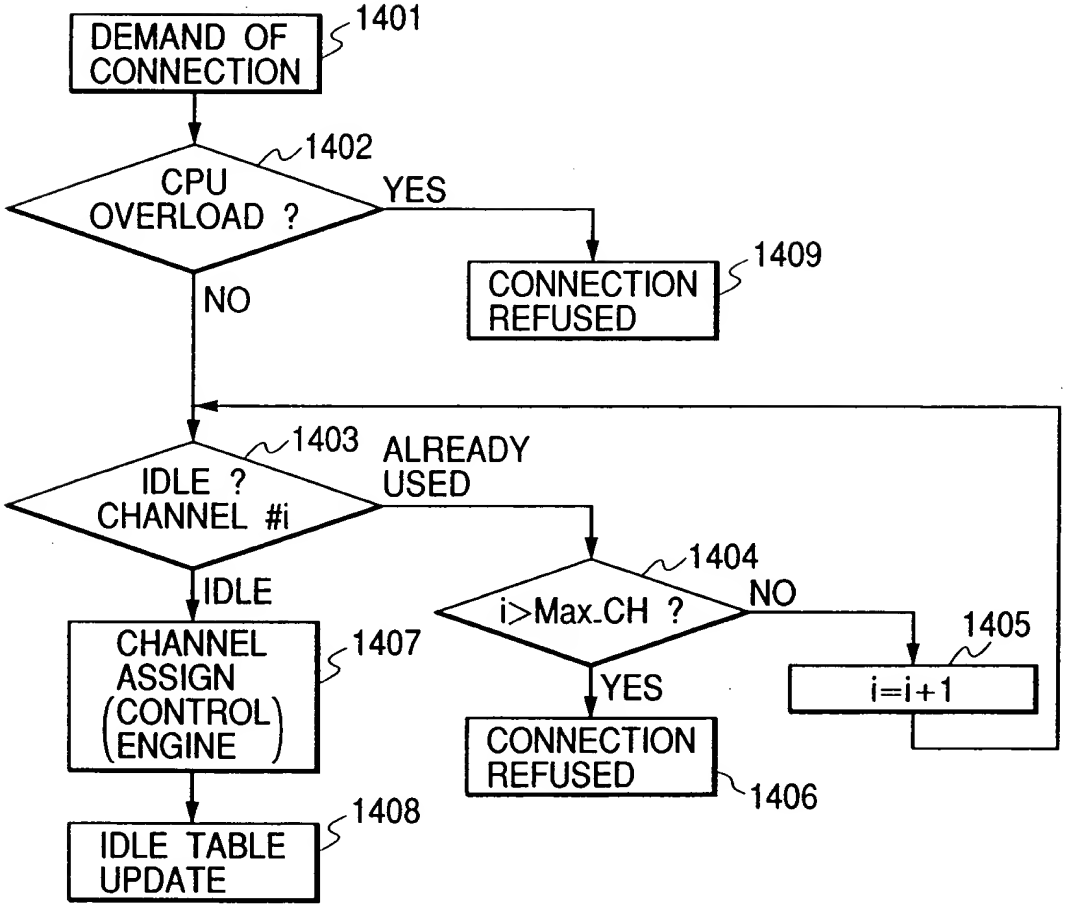

DEMAND OF CONNECTION
1401
CPU OVERLOAD ?
1402
YES
CONNECTION REFUSED
1409
NO
IDLE ? CHANNEL #i
1403
ALREADY USED
IDLE
i>Max_CH ?
1404
NO
1405
i=i+1
YES
CONNECTION REFUSED
1406
CHANNEL ASSIGN (CONTROL) ENGINE
1407
IDLE TABLE UPDATE
1408

FIG. 15

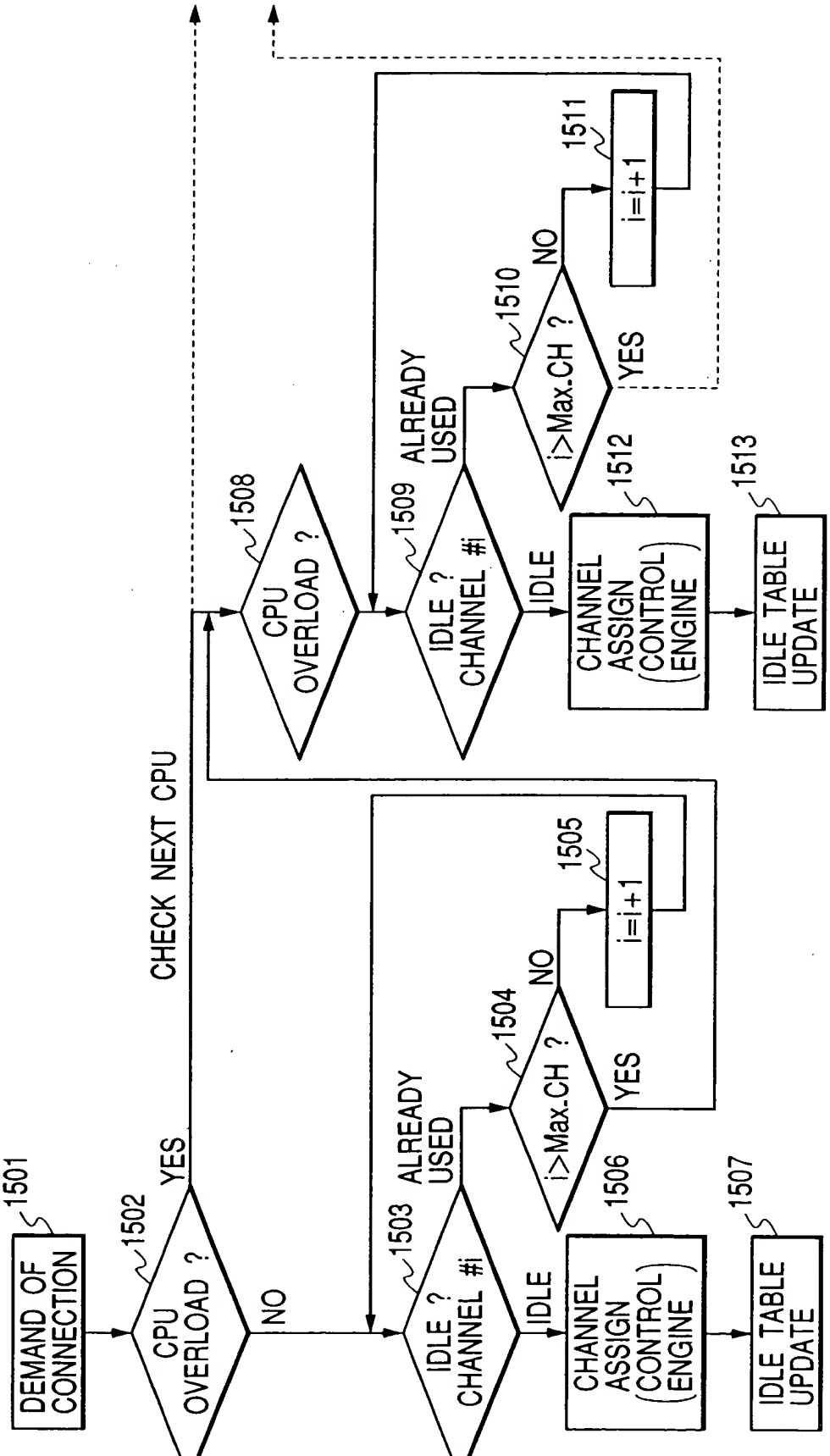

DEMAND OF CONNECTION
1501
CPU OVERLOAD ?
1502
YES
NO
CHECK NEXT CPU
IDLE ? CHANNEL #i
1503
ALREADY USED
i>Max.CH ?
1504
NO
YES
i=i+1
1505
CHANNEL ASSIGN (CONTROL) (ENGINE)
1506
IDLE TABLE UPDATE
1507
IDLE
CPU OVERLOAD ?
1508
IDLE ? CHANNEL #i
1509
ALREADY USED
i>Max.CH ?
1510
NO
YES
i=i+1
1511
CHANNEL ASSIGN (CONTROL) (ENGINE)
1512
IDLE TABLE UPDATE
1513
IDLE

FIG. 16

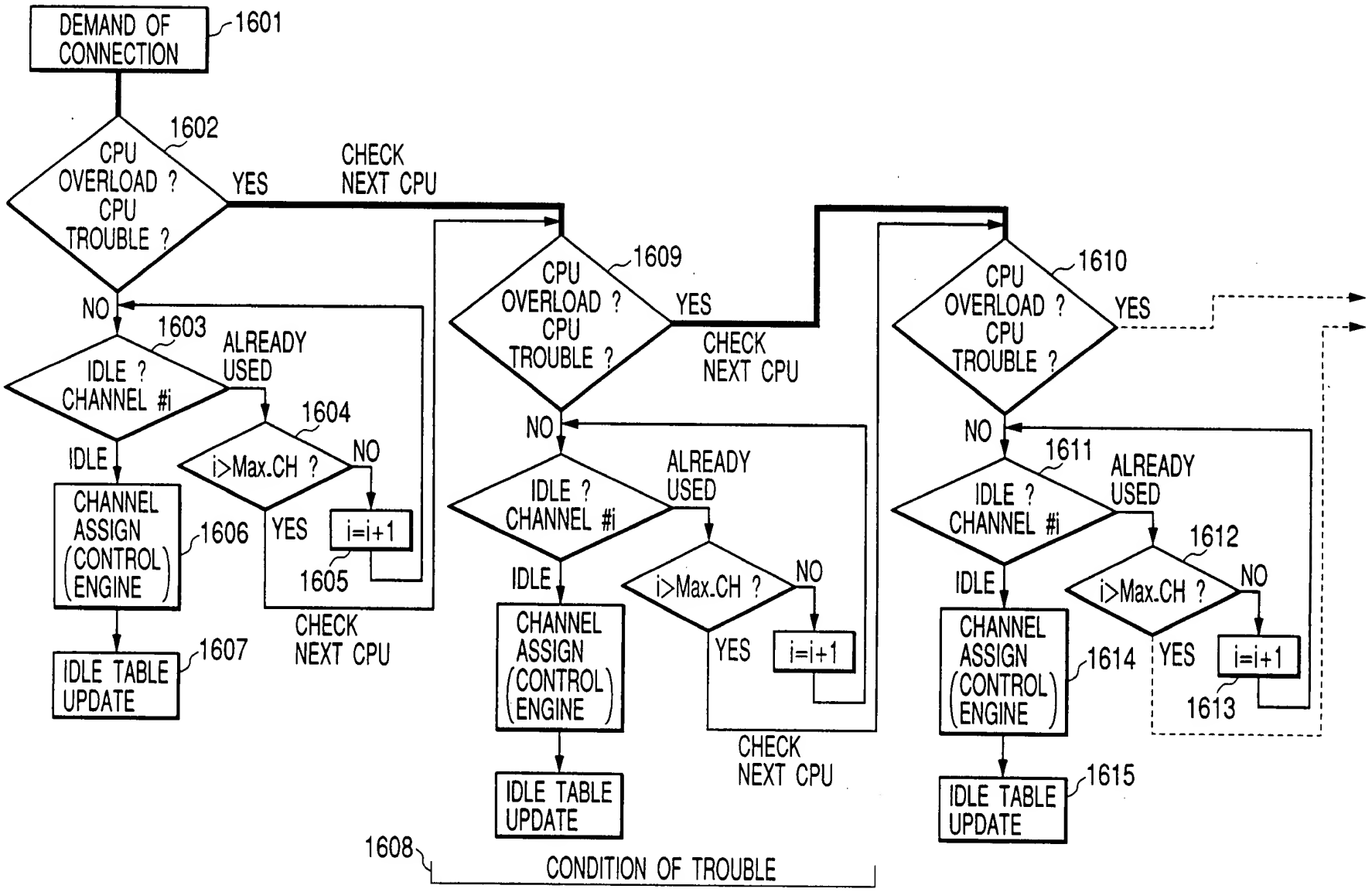

DEMAND OF CONNECTION
1601
CPU OVERLOAD ? CPU TROUBLE ?
1602
YES
CHECK NEXT CPU
NO
IDLE ? CHANNEL #i
1603
ALREADY USED
IDLE
i>Max.CH ?
1604
NO
YES
i=i+1
1605
CHECK NEXT CPU
CHANNEL ASSIGN (CONTROL ENGINE)
1606
IDLE TABLE UPDATE
1607
CPU OVERLOAD ? CPU TROUBLE ?
1609
YES
CHECK NEXT CPU
NO
IDLE ? CHANNEL #i
ALREADY USED
IDLE
i>Max.CH ?
NO
YES
i=i+1
CHECK NEXT CPU
CHANNEL ASSIGN (CONTROL ENGINE)
IDLE TABLE UPDATE
CPU OVERLOAD ? CPU TROUBLE ?
1610
YES
NO
IDLE ? CHANNEL #i
1611
ALREADY USED
IDLE
i>Max.CH ?
1612
NO
YES
i=i+1
1613
CHANNEL ASSIGN (CONTROL ENGINE)
1614
IDLE TABLE UPDATE
1615
1608
CONDITION OF TROUBLE

FIG. 17

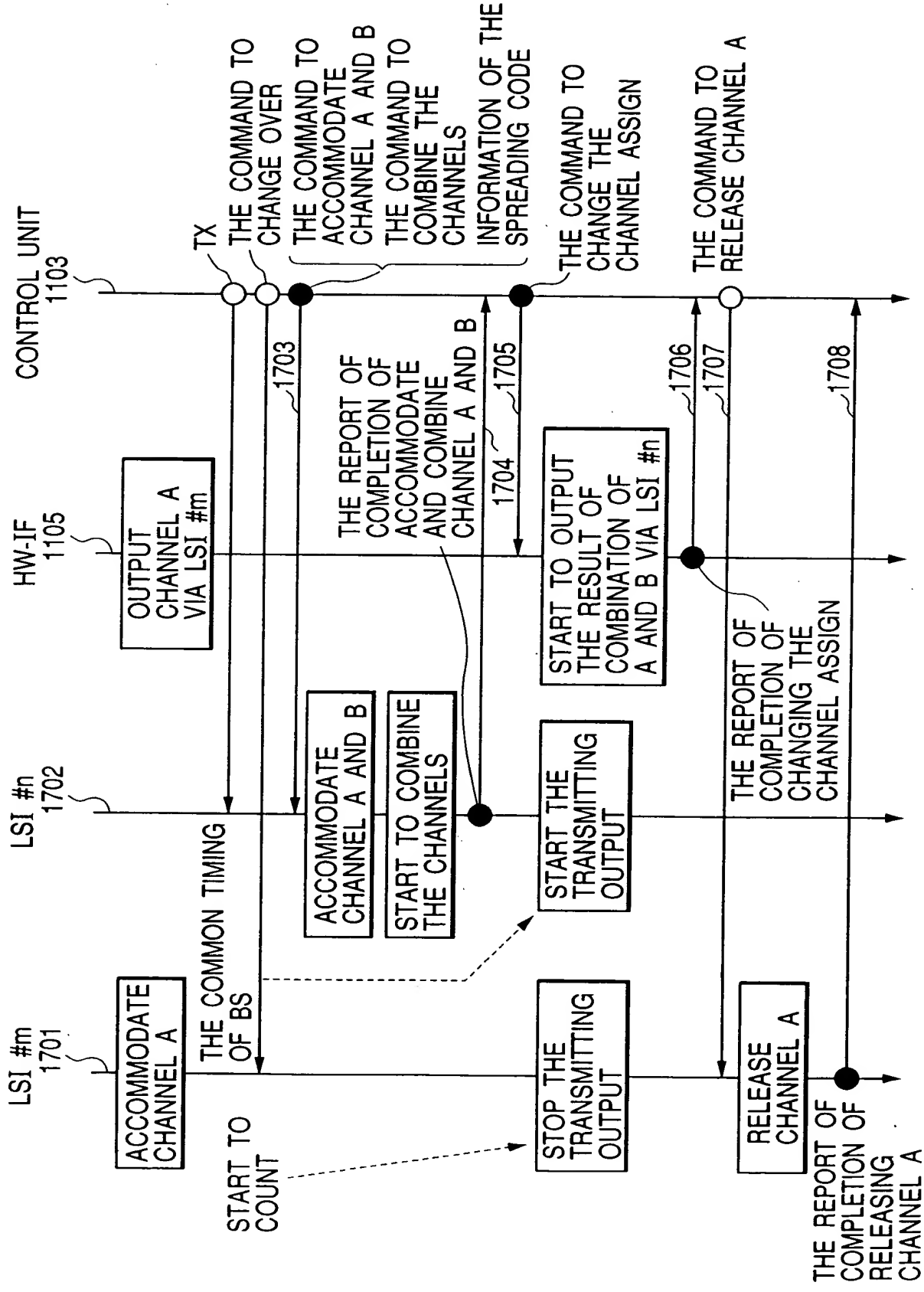

CONTROL UNIT
1103
HW-IF
1105
LSI #n
1702
LSI #m
1701
TX
THE COMMAND TO CHANGE OVER
THE COMMAND TO ACCOMMODATE CHANNEL A AND B
THE COMMAND TO COMBINE THE CHANNELS
INFORMATION OF THE SPREADING CODE
THE COMMAND TO CHANGE THE CHANNEL ASSIGN
THE COMMAND TO RELEASE CHANNEL A
OUTPUT CHANNEL A VIA LSI #m
1703
THE REPORT OF COMPLETION OF ACCOMMODATE AND COMBINE CHANNEL A AND B
1704
1705
1706
1707
1708
START TO OUTPUT THE RESULT OF COMBINATION OF A AND B VIA LSI #n
ACCOMMODATE CHANNEL A AND B
START TO COMBINE THE CHANNELS
START THE TRANSMITTING OUTPUT
THE REPORT OF COMPLETION OF CHANGING THE CHANNEL ASSIGN
ACCOMMODATE CHANNEL A
THE COMMON TIMING OF BS
START TO COUNT
STOP THE TRANSMITTING OUTPUT
RELEASE CHANNEL A
THE REPORT OF COMPLETION OF RELEASING CHANNEL A

FIG. 18

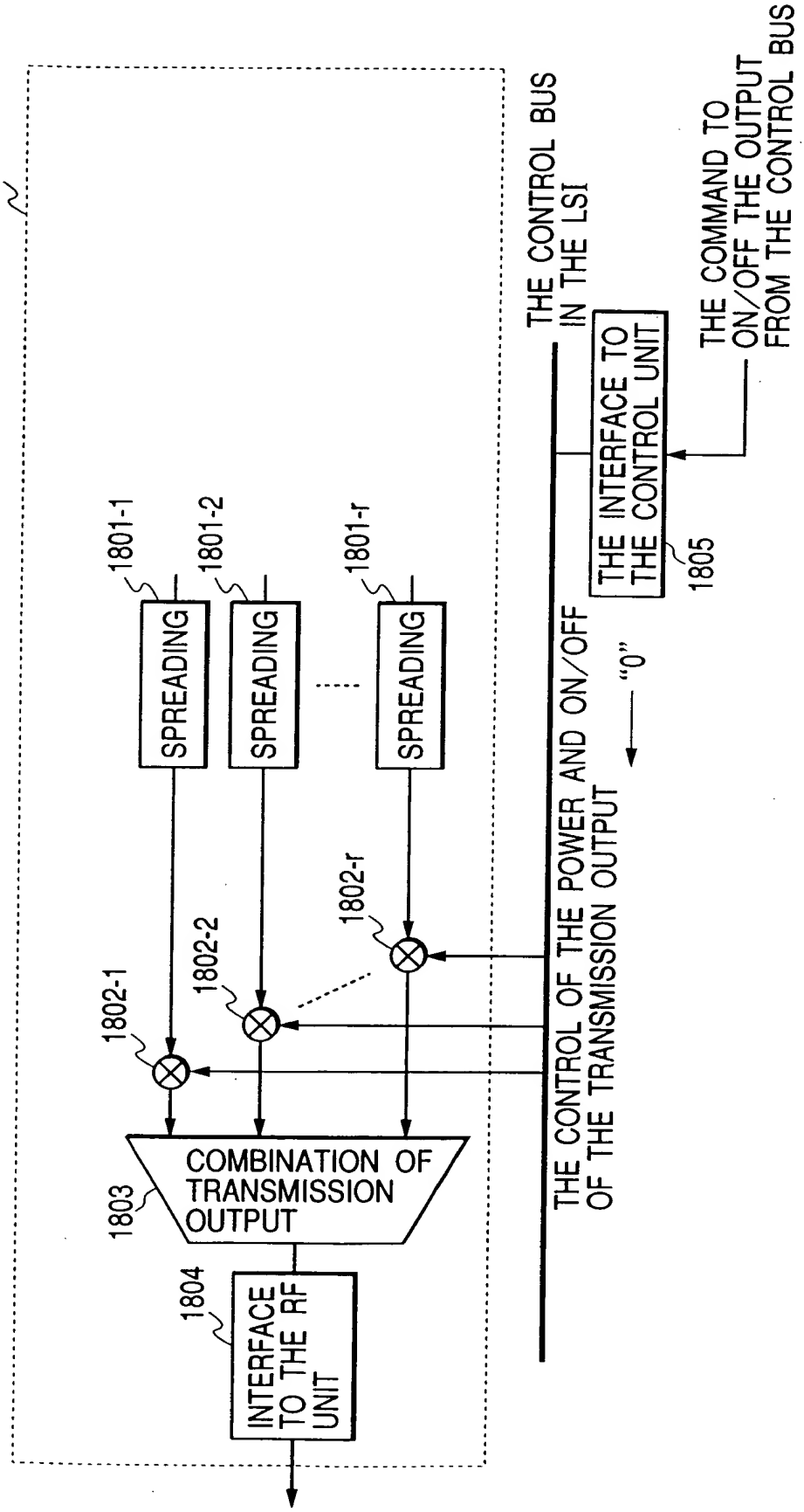
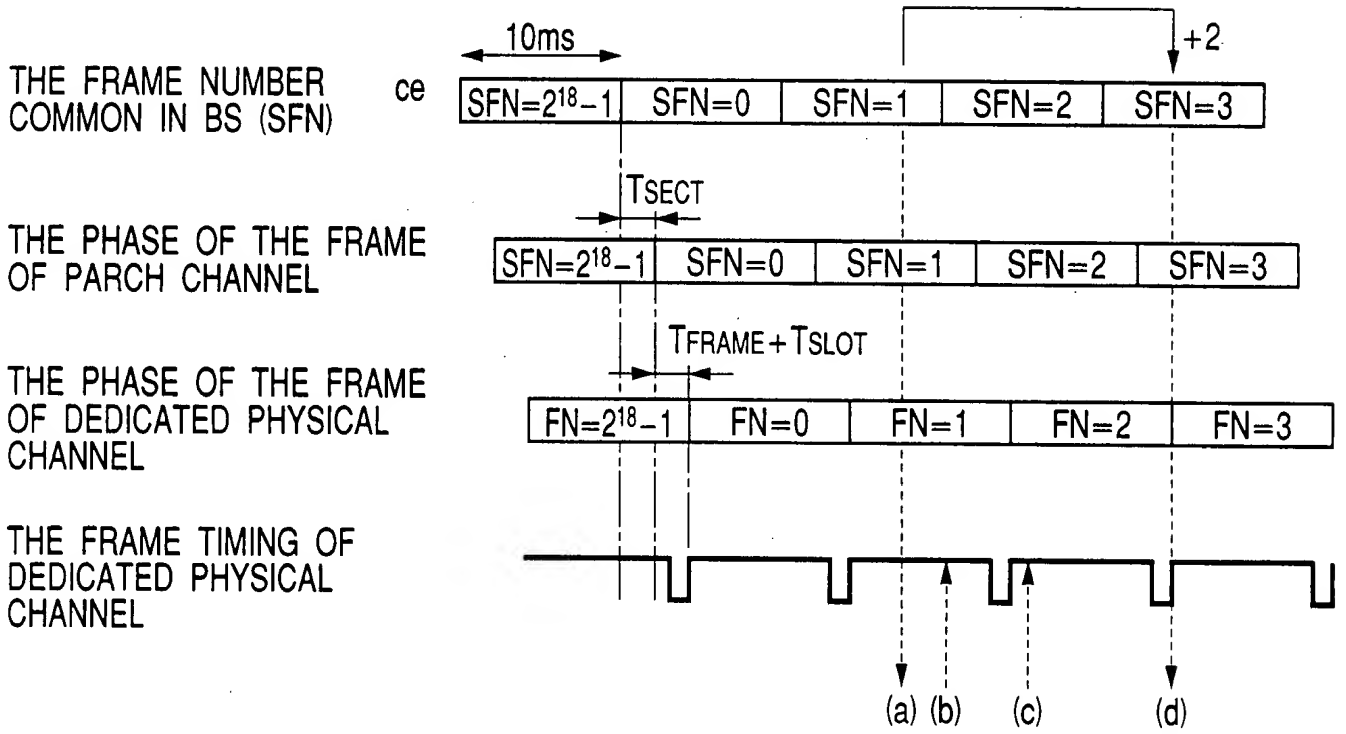

1101-m
THE CONTROL BUS IN THE LSI
THE COMMAND TO ON/OFF THE OUTPUT FROM THE CONTROL BUS
THE INTERFACE TO THE CONTROL UNIT
1805
1801-1
1801-2
1801-r
SPREADING
SPREADING
SPREADING
1802-1
1802-2
1802-r
"0"
THE CONTROL OF THE POWER AND ON/OFF OF THE TRANSMISSION OUTPUT
COMBINATION OF TRANSMISSION OUTPUT
1803
1804
INTERFACE TO THE RF UNIT

FIG. 19



(a) CONTROL UNIT DECIDES TO SWITCH THE CHANNELS, GET BS REFERENCE SFN, AND SEND THE COMMAND TO SWITCH

(b) THE COMMAND REACHES LSI #n

(c) THE COMMAND REACHES LSI #m

(d) EACH LSI EXECUTES THE SWITCHING

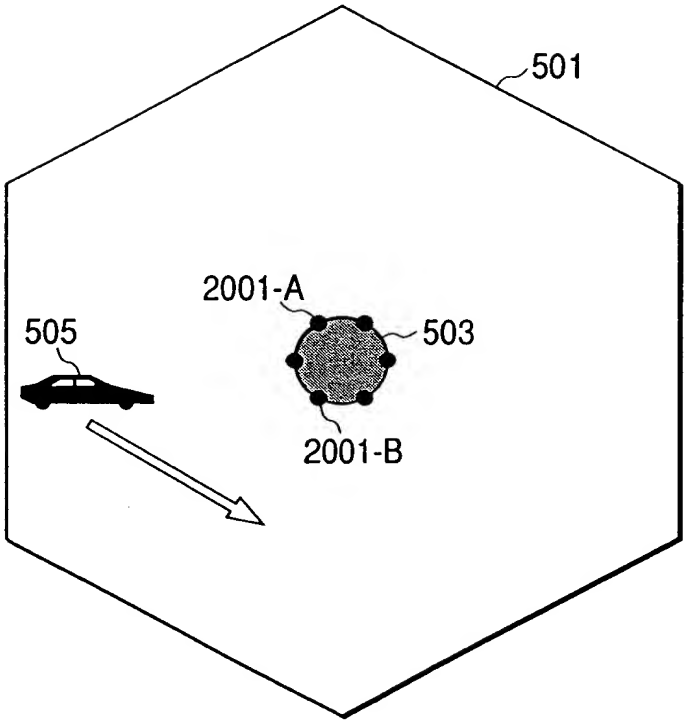



FIG. 20